UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,615	03/31/2004	Simon Knowles	66365-020	3818

7590 06/11/2008

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ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
06/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2008*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-18 and 21 have been considered. Claims 19-20 cancelled as per

Applicant's request. Claims 1-3, 5-6, 14-15, 18, and 21 have been amended as per

Applicant's request.

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-2, 5-7, 11, 14-16, 18, and 21 are rejected under 35 U.S.C. 102(b) as

being anticipated by Hull et al. (USPN 5,922,065, herein Hull).

2.   As per Claim 1, Hull teaches: A computer processor for processing (i) instruction

packets comprising a plurality of only control instructions (Figure 4, Template "B"), and

(ii) instruction packets comprising a plurality of instructions comprising at least one data

processing instruction (Figure 4, for example, Template "0"), the processor comprising:

        a decode unit for decoding sequentially the_instruction packets fetched from a

memory holding a sequence of instruction packets (Column 5, Lines 16-18);

        a control processing channel capable of performing control operations, the

control processing channel comprising a plurality of functional units (Column 3, Line 51,

the branch execution unit) including a control register file having a first bit width (Column

3, Lines 18-21); and

a data processing channel capable of performing data processing operations at

least one input of which is a vector, the data processing channel comprising a plurality

of functional units (Column 3, Lines 48-50, the integer, memory, and floating point

execution units) including a data register file having a second bit width wider than the

first bit width (Column 3, Lines 4-6, the data registers are 128 bits, the branch registers

are 64 bits);

wherein the decode unit comprises decode circuitry configured to decode

identification bits of each instruction packet to determine which type (i), (ii) of instruction

packet is being decoded, and control circuitry configured to pass the plurality of only

control instructions from an instruction packet of type (i) to the control processing

channel when the decode circuitry indicates so and to pass the plurality of instructions

comprising at least one data processing instruction from an instruction packet of type (ii)

to the data processing channel when the decode circuitry indicates so (Column 3, Lines

63-66, the template field in each packet/bundle tells the machine what is in each packet,

and directs the packet to the appropriate functional units. Template "B" for example

contains 3 branch (control) instructions, and Template "0" contains only data-processing

instructions);

wherein, in use the decode unit causes instructions of (i) instruction packets

comprising a plurality of only control instructions to be executed sequentially on the

control processing channel (Column 4, Lines 61-62); and

wherein in use the decode unit causes instructions of (ii) instruction packets

comprising a plurality of instructions comprising at least one data processing instruction

to be executed simultaneously on the data processing channel (Column 2, Lines 5-9).

3.   As per Claim 2, Hull teaches: A computer processor according to claim 1,

wherein the control processing channel further comprises a branch unit and a control

execution unit (Column 3, Line 51).

4.   As per Claim 5, Hull teaches: The computer processor according to claim 1,

wherein the control and data processing channels share a load store unit (Column 3,

Line 50, there is only one memory execution unit, and since the branch unit needs to be

able to have access to memory (to fetch the new target instructions), it clearly has to be

shared between the two).

5.   As per Claim 6, Hull teaches: A computer processor according to claim 5,

wherein the load store unit uses control information supplied by the control processing

channel and data supplied by the data processing channel (Column 3, Line 50, there is

only one memory execution unit, the data processing channel needs to use it to fetch

data from memory, and the control channel needs to use it to fetch branch target

addresses).

6.   As per Claim 7, Hull teaches: A computer processor according to claim 1,

wherein the instruction packets are all of equal bit length (Column 2, Lines 22-24, 128

bit bundles).

7.   As per Claim 11, Hull teaches: A computer processor according to claim 7,

wherein the nature of each instruction in an instruction packet is selected at least from a

control instruction, a data instruction, and a memory access instruction (Column 3,

Lines 48-51, also see Figure 4).

8.   As per Claim 14, Hull teaches: A computer processor according to claim 1,

wherein when the decode unit detects that the instruction packet defines three control

instructions, the decode unit is operable to supply the control processing channel with

the three control instructions (Column 3, Lines 65-66) whereby the three control

instructions are executed sequentially (Column 4, Lines 61-62).

9.   As per Claim 15, Hull teaches: A computer processor according to claim 1,

wherein when the decode unit detects that the instruction packet defines two

instructions comprising at least one data instruction, the decode unit is operable to

supply the second processing channel with at least the data instruction (Column 3,

Lines 65-66) whereby the two instructions are executed simultaneously (Column 2,

Lines 5-9).

10.   As per Claim 16, Hull teaches: A computer processor according to claim 1,

wherein the decode unit is operable to read the values of a set of designated bits at

predetermined bit locations in each instruction packet of the sequence (Column 3, Lines

63-66, the template bits), to determine:

a) whether the instruction packet defines a plurality of only control instructions

(Figure 4, Template "B") or a plurality of instructions of which at least one is a data

instruction (Figure 4, any non-"B" template); and

b) where the instruction packet defines a plurality of instructions of which at least

one is a data instruction, the nature of each of the two instructions selected from: a

control instruction; a data instruction; and a memory access instruction (Figure 4, see

Template "0" or "8" for example).

11.   As per Claim 18, Hull teaches: A method of operating a computer processor for

processing (i) instruction packets comprising a plurality of only control instructions

(Figure 4, Template "B"); and (ii) instruction packets comprising a plurality of instructions

comprising at least one data processing instruction (Figure 4, Template "0"),

the processor comprising a decode unit for decoding sequentially the instruction

packets fetched from a memory holding the instruction packets (Column 5, Lines 16-

18):

a control processing channels comprising a plurality of functional units (Column

3, Line 51, the branch execution unit) including a control register file having a first bit

width (Column 3, Lines 18-21) and a data processing channel comprising a plurality of

functional units including a data register file having a second bit width, wider than the

first bit width (Column 3, Lines 4-6, the data registers are 128 bits, the branch registers

are 64 bits), the method comprising:

decoding identification bits of each instruction packet to determine which type (i),

(ii), of instruction packet is being decoded, and passing the plurality of only control

instructions from an instruction packet of type (i) to the control processing channel when

the decode circuitry indicates so and passing the plurality of instructions comprising at

least one data processing instruction from an instruction packet of type (ii) to the data

processing channel when the decode circuitry indicates so (Column 3, Lines 63-66, the

template field in each packet/bundle tells the machine what is in each packet, and

directs the packet to the appropriate functional units. Template "B" for example contains

3 branch (control) instructions, and Template "0" contains only data-processing

instructions);

when the instruction packet defines (i) a plurality of only control instructions,

supplying the control instructions to the control processing channel wherein the control

instructions are executed sequentially (Column 4, Lines 61-62); and

when the instruction packet defines (ii) a plurality of instructions comprising at

least one data processing instruction, supplying at least the data instruction to the data

processing channel wherein the plurality of instructions are executed simultaneously

(Column 2, Lines 5-9).

12.   As per Claim 21, Hull teaches: A computer-readable medium comprising a

sequence of instruction packets (Column 2, Lines 22-24),

        said instruction packets including a first type of instruction packet comprising a

plurality of only control instructions of substantially equal length (Figure 4, Template "B")

and a second type of instruction packet comprising a plurality of instructions including at

least one data instruction (Figure 4, Template "0"),

        said instruction packets including at least one indicator bit at a designated bit

location within the instruction packet (Column 3, Lines 63-66, the template fields),

wherein the computer-readable medium is adapted to run on a computer such that said

indication bit is adapted to cooperate with a decode unit of the computer to designate

whether:

        a) the instruction packet defines a plurality of only control instructions or a

plurality of instructions comprising at least one is a data instruction (Column 3, Lines 63-

66); and

        b) in the case when there is a plurality of instructions comprising at least one

data instruction, the nature of each of the first and second instructions selected from: a

control instruction; a data instruction; and a memory access instruction (Figure 4, see

Templates "0" or "8" for example).

Claim Rejections - 35 USC § 103

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14.   Claims 3, 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, in view of "Unifying FPGAs and SIMD Arrays" by Bolotski et al. (herein Bolotski).

15.   As per Claim 3, Hull teaches The computer processor according to claim 1, wherein the data processing channel further comprises a fixed data execution unit (Column 3, Lines 48-51), but fails to teach:

the second processing channel containing a configurable data execution unit.

While Hull teaches a fixed data execution unit, Hull is silent towards a configurable data execution unit. However, Bolotski teaches a system that can simulate SIMD and configurable operations on the same unit (Section 4), which can be subdivided until SIMD and configurable units. Boloski further teaches that the advantages of combining a SIMD and configurable unit includes reducing cost by not duplicating logic (Section 4.1), additionally, one of ordinary skill in the art would recognize the additional benefits of configurable hardware, such as being able to configure exactly the units you need, allowing for flexibility and increased performance. Therefore, one of ordinary skill in the art would have been motivated to combine the teachings of Hull and Bolotski to implement configurable data execution units.

16.   As per Claim 4, Bolotski teaches: A computer processor according to claim 3,

wherein the fixed data execution unit and the configurable data execution unit both

operate according to a single instruction multiple data format (Section 4).

17.   As per Claim 17, Hull teaches: A computer processor according to claim 3,

wherein the configurable data execution unit is capable of executing more than two

consecutive operations on the data provided by a single issued instruction before

returning a result to a destination register file.

        One of ordinary skill in the pertinent art would have recognized that this is a

simple accumulate function that would be easily programmable in configurable logic.

18.   Claims 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Hull, in view of In re Rose.

19.   These claims recite limitations of the bit lengths of various instructions and

packets.

        While Hull may not teach the recited lengths, if it was advantageous to lengthen

or shorten the bit lengths in Hull for various reasons, one of ordinary skill in the pertinent

art would have recognized that it would have been simple to do so.

        Further, it has been found that a change in size does not produce a patentable

distinction. In re Rose , 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to

a lumber package "of appreciable size and weight requiring handling by a lift truck"

where held unpatentable over prior art lumber packages which could be lifted by hand

because limitations relating to the size of the package were not sufficient to patentably

distinguish over the prior art.); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA

1976) ("mere scaling up of a prior art process capable of being scaled up, if such were

the case, would not establish patentability in a claim to an old process so scaled." 531

F.2d at 1053, 189 USPQ at 148.).

Response to Arguments

3.   In light of the Applicant's amendments to Claims 1, 18, and 21 (the independent

claims), and further in light of the arguments presented, Examiner agrees that the

claims as currently presented have overcome Kahle. However, upon a further search of

the new claims, Examiner has found a new reference, Hull, which has been applied

above. As a result of the new grounds of rejection in light of the new reference, the

Applicants arguments towards the rejection are moot.

Conclusion

4.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

        A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to ROBERT E. FENNEMA whose telephone number is

(571)272-2748. The examiner can normally be reached on Monday-Friday, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/   Robert E Fennema

Supervisory Patent Examiner, Art Unit 2183   Examiner
                                                    Art Unit 2183

RF